# POWER DISTRIBUTION SYSTEM, METHOD, AND LAYOUT FOR AN ELECTRONIC DEVICE

## Background of the Invention

The present invention relates in general to power distribution on an electronic device such as, for example, an integrated circuit or printed circuit board.

In designing the layout for a semiconductor integrated circuit, there is often a need to place identical circuit blocks next to each other. This is typically done by preparing the layout for a master circuit block (e.g., containing several thousands of transistor devices), placing the master circuit block layout within the overall chip layout for the integrated circuit, and then creating and placing identical (i.e., mirror or symmetrical) images of the master circuit block on the integrated circuit layout next to the master circuit block. Several such image circuit blocks may be formed depending on the particular integrated circuit design. One of the reasons that such image circuit blocks are formed is so that input/output pins to each circuit block can be placed on the layout so that they are opposite one another to reduce the layout area required and the layout routing distance necessary to connect the input/output pins to the rest of the integrated circuit.

In placing the master and image circuit blocks, care is generally taken to ensure that input/output signals and power supply connections common to the master and image circuit blocks are implemented in a way within the overall layout design so that routing congestion is minimized and signal timing and power supply parasitics are balanced and within acceptable variations for the master and image circuit blocks.

Prior layout approaches include the use of VDD and VSS power rings within each of the master and image circuit blocks. However, the use of such power rings consumes a large amount of layout area in part due to redundancy in the resulting power supply distribution grid across the integrated circuit. Prior overall chip layout design approaches further have not integrated the use of such power rings into a

comprehensive and layout-efficient, top-down power distribution layout methodology. Instead, prior approaches typically defer full-chip power integration to the end of the layout process, which results in inefficient usage of layout area for power distribution needs.

In light of the foregoing, there is a need for an improved power distribution system for an integrated circuit layout that more efficiently uses the layout area required for providing power to master and image circuit blocks and other circuits in the integrated circuit. There is a further need for such a power distribution system that readily integrates with a top-down layout design and integration process for completing the overall circuit layout and power distribution design of the integrated circuit.

## Brief Description of the Drawings

For a more complete understanding of the present invention, reference is now made to the following figures, wherein like reference numbers refer to similar items throughout the figures:

FIG. 1 is a layout view of a power distribution structure according to the present invention;

FIG. 2 is a layout view of master and image circuit blocks coupled to a power distribution structure according to the present invention;

FIG. 3 is a layout plan for a full integrated circuit chip using a plurality of power distribution structures according to the present invention; and

FIG. 4 is the layout plan of FIG. 3 showing the placement of master and image circuit blocks coupled to the power distribution structures.

## Detailed Description of the Drawings

FIG. 1 is a layout view of a power distribution structure 100 according to the present invention. Structure 100 comprises a power line 102 for providing a first power supply voltage such as, for example, a positive supply voltage VDD, and power lines

104 and 106 for providing a second power supply voltage such as, for example, VSS or ground. The overall layout of structure 100 is symmetrical about a central symmetry axis 108 for ease in overall layout design and integration when structure 100 is incorporated into and coupled to circuit blocks as will be discussed further below. It should be noted that the relative ordering of VDD and VSS could be switched if desired so that power line 102 provides a voltage VSS and power lines 104 and 106 provide a voltage VDD.

Power line 102 has a line width w2 and power lines 104 and 106 have a line width w1. As will be discussed further below, structure 100 will extend over large portions of an integrated circuit layout running distances of, for example, 50 microns and greater. Because a single power line 102 is used to supply VDD and two power lines 104 and 106 of substantially identical shape are used to supply VSS, the width w2 is preferably about twice the width w1. However, this ratio could vary for specific designs. The separation distance d between power line 102 and power lines 104 and 106 is preferably substantially equal to maintain the symmetrical layout of structure 100.

It should be noted that structure 100 is illustrated as a triplet structure with three power lines. However, in other designs additional power lines could be used. It is preferable that such additional power lines also exhibit substantial symmetry about axis 108.

FIG. 2 is a layout 200 of master and image circuit blocks coupled to a power distribution structure according to the present invention. Specifically, a master circuit block 202 and image circuit block 204 are disposed, for example, in the layout plan of an integrated circuit. However, it should be noted that the present invention is also applicable to the design of power distribution layouts for other electronic devices such as printed circuit board assemblies having many chips to be mounted on a printed circuit board. For printed circuit board assemblies (not shown), the circuit blocks to be mirrored would correspond to entire integrated circuit chips oriented to be symmetrical about a symmetry axis on the printed circuit board layout.

The term "block" as used herein generally refers to a related group of transistors and/or other electronic elements that, for example, implement specific logical or other functions for the integrated circuit or other electronic device. Master circuit block 202 is used as a master in creating an identical, but mirrored circuit layout for image circuit block 204. By mirroring the circuit layout, input/output pins 212 and 214 for each circuit block are disposed facing opposite one another in layout 200. The mirroring is done about symmetry axis 206. This basic process of forming a master and image circuit blocks may be repeated many times for different portions of an integrated circuit design.

Power distribution structures 208 and 210 run across layout 200 and are electrically coupled to and run across master and image circuit blocks 202 and 204. Although shown in simplified form for purposes of illustration, structures 208 and 210 may use, for example, structure 100 of FIG. 1 as the basic unit for layout across the full semiconductor chip. Blocks 202 and 204 may have sizes that vary, for example, from about 100 by 100 microns to 1,000 by 1,000 microns and larger. Also, the shape of blocks 202 and 204, although typically square or rectangular, may also vary for specific designs.

FIG. 3 is a layout plan 300 for a full integrated circuit chip 302 using a plurality of power distribution structures (e.g., structures 304, 306, and 308) spread across the surface of chip 302 to provide an overall power distribution system for providing supply voltages to circuits (illustrated in FIG. 4) on chip 302. These structures are formed, for example, in a top metal layer of the integrated circuit. According to the present invention, a common symmetrical power distribution structure such as structure 100 of FIG. 1 is repeated to form many such structures, spaced substantially evenly, to run across preferably the entire, or at least a substantial portion, of the layout for chip 302. The repeated structures, including, for example, structures 304, 306 and 308, are spaced with a pitch P, for example, of 100 microns. However, pitch P can vary widely and be optimized for specific layout and chip designs based on factors such as the predominant circuit block size to be incorporated into the integrated circuit.

Each of structures 304, 306, and 308 and the other similar repeated structures that may be disposed across chip 302 run substantially in parallel with each other and are, for example, connected to power distribution rings 310 and 312 running around the perimeter of chip 302. Each of distribution rings 310 and 312 is respectively connected to a power supply voltage pad 314 and 316 for coupling to external power supply sources that provide, for example, VDD and VSS potentials. It will be appreciated that many other forms of distribution rings and other structures may be used to electrically couple the repeating, symmetrical power distribution structures of the present invention to external power supply sources for chip 302. Rings 310 and 312 will generally have a line width that is greater than that of the power lines of structures 304, 306, and 308.

FIG. 4 is a layout plan 400 including the layout plan 300 of FIG. 3 with the addition of master and image circuit blocks coupled to the repeated power distribution structures. Specifically, a master block 402 and image block 404 are placed in layout plan 400 and are electrically coupled to the repeated power structures 304, 306, 308 and 405. Pins 408 and 410 are used for input/output signals to each block. Master circuit block 402 contains, for example, a logic circuit 406 coupled to receive power through structure 308. This is typical and each circuit block may contain many such logic circuits.

It should be noted that according to the present invention master and image blocks 402 and 404 are placed within layout plan 400 so that an offset O1 from a boundary of the perimeter of each block to a corresponding power distribution structure is substantially equal. According to the present invention, this equal offset in combination with an even pitch P results in the relative position of the power distribution system to the circuitry (not shown) within each block being substantially the same for either the master or image blocks.

Other circuit blocks such as block 434 may also be placed in layout plan 400, even though there is no corresponding image block, and coupled to the power distribution structure 436. Also, a higher-level or super-block 420, having input/output signal pins 422, may contain a master block 424 and several image blocks 426, 428, and

430 all placed with a substantially equal offset O2 from corresponding power distribution structures. It should be noted that smaller blocks, for example master and image blocks 424 and 426 and also image blocks 428 and 430, may have a power distribution structure 432 disposed between them that is not electrically connected to either master block 424 or its image blocks.

According to a method of the present invention, a power distribution system is built in a top-down manner in which symmetrical power distribution structures are placed and spread evenly across chip 302 with a constant pitch P prior to the placement of individual master and image circuit blocks. The pitch P may be varied for differing circuit block sizes. For example, the pitch P may be made smaller if the predominant circuit block size is smaller. The structures 100 are substantially linear, each running substantially in parallel for distances of, for example, 50 microns or greater.

Next, after preparing the foregoing overall power distribution system layout, the master and image circuit blocks are added to and placed within the layout using a substantially constant offset from the block boundary to respective power distribution structures as described above. It should be noted that according to the present invention, power rings and other general power distribution schemes are typically not added to the master and image circuit blocks prior to integration into the overall chip layout. Instead, generally after placing the master and image circuit blocks within the overall layout power integration, electrical coupling of circuitry within each circuit block is provided.

According to the layout method above, the power distribution structures themselves are preferably not flipped or mirrored when forming image blocks because in general there is not a need to do this. Instead, the power distribution grid is first defined globally for chip 302 and then the master and image blocks formed and coupled to it. It should be noted that according to the present invention, the symmetrical layout of power distribution structure 100 aids in this layout design method. For example, when electrical connections are made in layout between circuitry and distribution structures 100 within a master block, the mirror image of the master block with its

individual circuitry power connections will correspondingly match up to the other parallel distribution structure or structures used to power the image circuit block. Because of the symmetry of structures 100, the final layout of the circuit block and the corresponding structures 100 connected to it will be a mirror image just as if all circuitry and power lines running across a master block were actually flipped or mirrored.

By the foregoing description, a novel method and system for a power distribution system for an electronic device have been described. The present invention has the advantages of more efficiently using the layout area required for providing power to master and image circuit blocks and other circuits in an integrated circuit. Also, the present invention provides a top-down layout design and integration process for completing the overall circuit layout and power distribution design of the integrated circuit to use chip area in a more efficient manner.

Although specific embodiments have been described above, it will be appreciated that numerous modifications and substitutions of the invention may be made. Accordingly, the invention has been described by way of illustration rather than limitation.